

REMARKS

Claims 1-28 are pending in the Application. Claims 1-3 and 12-14 are rejected under 35 U.S.C. §102(e). Claims 7 and 16-18 are rejected under 35 U.S.C. §103(a). Claims 4-6, 8-11, 15 and 19-22 are objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 23-28 are allowed. Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request that the Examiner reconsider and withdraw these rejections.

I. REJECTIONS UNDER 35 U.S.C. § 102(b):

The Examiner has rejected claims 1-3 and 12-14 under 35 U.S.C. § 102(b) as being anticipated by Antosik (U. S. Patent No. 6,822,975). Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request the Examiner to reconsider and withdraw these rejections.

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. § 2131.

Applicants respectfully assert that Antosik does not disclose "a port scanning unit for extracting data from the data signals received by said ports, characterized in that said port scanning unit is configured to extract data from ports providing data streams having at least two different input data rates" as recited in claim 1 and similarly in claim 12. The Examiner cites element 122 in Figure 1 of Antosik as disclosing a port scanning unit and column 3, lines 2-24 of Antosik as disclosing the above-cited claim limitation. Paper No. 3, page 2. Applicants respectfully traverse and assert that Antosik instead discloses that the node (referring to element 1 in Figure 1) is configured with a multiplexer (element 122 in Figure 1) that combines up to eight different OC3/OC12-rate electrical signals into an OC48-rate electrical signal. Column 5, lines 20-24. Antosik further discloses that the mux is configured to combine two or more incoming electrical signals into an electrical signal where at least one incoming electrical signal has a first frame format at a first data rate and at

least one other incoming electrical signal has a second frame format at a second data rate greater than the first data rate. Column 3, lines 2-8. Hence, Antosik discloses a multiplexer that combines two or more incoming electrical signals into an electrical signal where the incoming electrical signals may have a different data rate. However, combining two electrical signals is not the same as extracting data from the data signals. Thus, Antosik does not disclose all of the limitations of claims 1 and 12, and thus Antosik does not anticipate claims 1 and 12. M.P.E.P. §2131.

Claims 2-3 and 13-14 each recite combination of features including the above combinations, and thus are not anticipated for at least the above-stated reasons. Claims 2-3 and 13-14 recite additional features which, in combination with the features of the claims upon which they depend, are not anticipated by Antosik.

For example, Antosik does not disclose "a control logic unit functionally connected to said port scanning unit for determining which of said at least two ports need to be handled within which clock cycle with regard to its input data rate" as recited in claim 2 and similarly in claim 13. The Examiner cites Figure 15 of Antosik as disclosing a control logic unit and element 122 in Figure 1 of Antosik as disclosing a port scanning unit. Paper No. 3, page 2. The Examiner further cites column 23, line 37 – column 25, line 40 of Antosik as disclosing the above-cited claim limitation. Paper No. 5, page 2. Applicants respectfully traverse.

Antosik instead discloses that Figure 15 discloses a block diagram of a muxing/demuxing circuit for the mux/demux board of a node. Column 23, lines 22-23. Antosik further discloses transceiver circuitry with appropriate clock-and-data-recovery (CDR) circuitry that recovers up to eight different customer signal clocks from the up to eight different OC3/OC12-rate incoming customer signals. Column 23, lines 53-57. Antosik further discloses that the customer signal clocks generated from OC3 signals have a clock rate of 155 MHZ, while customer signal clocks generated from OC12 signals have a clock rate of 622 MHZ. Column 23, lines 57-59.

Applicants respectfully request the Examiner to particularly point out in Figure 15 which element allegedly discloses a control logic unit pursuant to 37 C.F.R. §1.104(c)(2). Furthermore, there is no depiction in Figure 15 of element 122 which the Examiner asserts allegedly discloses a port scanning unit. Hence, Antosik does

not disclose a control logic unit functionally connected to a port scanning unit. Further, Antosik discloses generating customer signal clocks with different clock rates. This is not the same as determining which of the ports need to be handled within which clock cycle. Neither is the same as determining which of the ports need to be handled within which clock cycle with regard to its input data rate. Thus, Antosik does not disclose all of the limitations of claims 2 and 13, and thus Antosik does not anticipate claims 2 and 13. M.P.E.P. §2131.

Applicants further assert that Antosik does not disclose "wherein the control logic unit is configured to control said port scanning unit to access a port having a higher input data rate proportionally more often than a port having a lower input data rate" as recited in claim 3 and similarly in claim 14. The Examiner cites column 23, line 37 – column 25, line 40 as support that Antosik inherently discloses the above-cited claim limitation. Paper No. 5, page 3. Applicants respectfully traverse.

As stated above, Antosik instead discloses generating customer signal clocks with different clock rates. The Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that generating customer signal clocks with different clock rates inherently discloses controlling a port scanning unit (Examiner asserts that element 122 of Figure 1 of Antosik allegedly discloses a port scanning unit) to access a port having a higher input data rate proportionally more often than a port having a lower input data rate. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that generating customer signal clocks with different clock rates inherently discloses controlling a port scanning unit to access a port having a higher input data rate proportionally more often than a port having a lower input data rate, and that it would be so recognized by persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Since the Examiner has not provided such evidence, the Examiner is merely relying upon his own subjective opinion which is insufficient to establish a *prima facie* case of anticipation. *See In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002); M.P.E.P. §2131. Thus, Antosik does not disclose all of the limitations of claims 3 and 14, and thus Antosik does not anticipate claims 3 and 14. M.P.E.P. §2131.

As a result of the foregoing, Applicants respectfully assert that not each and every claim limitation was found within Antosik, and thus claims 1-3 and 12-14 are not anticipated by Antosik.

II. REJECTIONS UNDER 35 U.S.C. §103(a):

The Examiner has rejected claims 7 and 16-18 under 35 U.S.C. §103(a) as being unpatentable over Antosik in view of Goodman (U.S. Patent No. 6,636,529). Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request the Examiner to reconsider and withdraw these rejections.

A. The Examiner has not provided any objective evidence or source of motivation for combining Antosik with Goodman.

A *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. §2142. The showings must be clear and particular and supported by objective evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

The Examiner admits that Antosik does not teach have a central buffer connected to a port scanning unit into which data from all ports are written, as recited in claim 7 and similarly in claim 18. Paper No. 3, page 3. The Examiner's motivation for modifying Antosik with Goodman to have a central buffer connected to a port scanning unit into which data from all ports are written, as recited in claim 7 and similarly in claim 18, is "to prevent data loss." Paper No. 3, page 3. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner has not presented a source for his motivation for modifying Antosik with Goodman. The Examiner simply states "to prevent data loss" as

motivation for modifying Antosik with Goodman to have a central buffer connected to a port scanning unit into which data from all ports are written. The motivation to modify Antosik with Goodman must come from one of three possible sources: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453, 1457-58 (Fed. Cir. 1998). The Examiner has not provided any evidence that his motivation comes from any of these sources. Instead, the Examiner is relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 7 and 18. *Id.*

Furthermore, the Examiner's motivation does not address as to why one of ordinary skill in the art with the primary reference (Antosik) in front of him would modify Antosik by connecting to the multiplexer (element 122 of Figure 1 of Antosik which the Examiner asserts as allegedly teaching a port scanning unit) a central buffer into which data from all ports are written in light of the teachings of the secondary reference (Goodman). Antosik teaches a multiplexer in a node in an optical communication network that combines two or more incoming electrical signals into an electrical signal where the incoming electrical signals may have a different data rate. Column 3, lines 2-8. Goodman, on the other hand, teaches that the disadvantage of a router or bridge is the complexity of processing the layer 2/3 information and the buffering of packets intended for various destinations. Column 2, lines 47-51. Goodman further teaches that the invention relates to interfaces for converting an incoming digital signal into a format for transmission on a synchronous digital network. Column 1, lines 23-25. The Examiner has not provided any objective evidence as to why one of ordinary skill in the art would modify Antosik, which teaches combining two or more incoming electrical signals into an electrical signal where the incoming electrical signals may have a different data rate, with Goodman, which teaches converting an incoming digital signal into a format for transmission on a synchronous digital network. That is, the Examiner has not provided any objective evidence as to why one of ordinary skill in the art would modify Antosik to connect

to the multiplexer (element 122 of Figure 1 of Antosik) a central buffer into which data from all ports are written in view of Goodman, which teaches converting an incoming digital signal into a format for transmission on a synchronous digital network. The Examiner is merely relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 7 and 18. *Id.*

B. The Examiner has not provided any motivation for combining Antosik with Goodman to include the limitations of claims 16 and 17.

The Examiner has not presented any motivation for modifying Antosik with Goodman to temporarily store data, as recited in claim 16. Further, the Examiner has not presented any motivation for modifying Antosik with Goodman to temporarily store data according to the FIFO concept with a speed corresponding to the input data rate of the connected port, as recited in claim 17. The Examiner must provide a motivation or suggestion to modify Antosik with Goodman to include above-stated limitations. M.P.E.P. §2142. Since the Examiner has not provided any motivation, the Examiner has not provided a *prima facie* case of obviousness for rejecting claims 16-17. *Id.*

C. The Examiner has not presented a reasonable expectation of success when combining Antosik with Goodman.

The Examiner must present a reasonable expectation of success in combining Antosik with Goodman in order to establish a *prima facie* case of obviousness. M.P.E.P. §2143.02.

As stated above, Antosik teaches a multiplexer in a node in an optical communication network that combines two or more incoming electrical signals into an electrical signal where the incoming electrical signals may have a different data rate. Column 3, lines 2-8

Goodman, on the other hand, teaches a FIFO (element 490 in Figure 4) that receives inter-packet data for retiming. Column 10, lines 1-2. Goodman further

teaches that the FIFO bridges the domain of the data clock based on the incoming data signal and the SDH container clock. Column 10, lines 2-4.

Based on Applicants understanding, the Examiner asserts that element 490 of Goodman teaches a central buffer. As further understood by the Applicants, the Examiner asserts that element 122 of Antosik teaches a port screening unit. The Examiner admits that Antosik does not teach a center buffer connect to the port screening unit into which data from all ports are written. Paper No. 3, page 3. The Examiner asserts that this missing limitation is found in Goodman. Paper No. 3, page 3. By the Examiner asserting that element 490 of Goodman teaches a central buffer, the Examiner has effectively connected the FIFO (element 490) of Goodman, which resides in a linecode recognition and mapping block of a SDH framing device, to the multiplexer (element 122) of Antosik, which resides in a node in an optical communication network. Column 9, lines 48-49 of Goodman; Column 4, lines 33-36 of Antosik.

The Examiner has not presented any evidence that there would be a reasonable expectation of success in connecting the FIFO (element 490) of Goodman, which resides in a linecode recognition and mapping block of a SDH framing device, to the multiplexer (element 122) of Antosik, which resides in a node in an optical communication network. The Examiner must provide objective evidence as to how a FIFO residing in a linecode recognition and mapping block of a SDH framing device would be connected to a multiplexer residing in a node in an optical communication network. M.P.E.P. §2143.02. Since the Examiner has not provided such evidence, the Examiner has not presented a reasonable expectation of success in combining Antosik with Goodman. M.P.E.P. §2143.02. Accordingly, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 7 and 16-18. M.P.E.P. §2143.02.

D. Antosik and Goodman, taken singly or in combination, do not teach or suggest the following claim limitations.

Applicants respectfully assert that Antosik and Goodman, taken singly or in combination, do not teach or suggest "a central buffer connected to said port scanning

unit into which data from all ports are written" as recited in claim 7 and similarly in claim 18. The Examiner cites column 9, line 50 – column 10, line 13 and Figure 14 of Goodman as teaching the above-cited claim limitation. Paper No. 3, page 3. Applicants respectfully traverse and assert that Goodman instead teaches a FIFO (element 490) that bridges the domain of the data clock based on the incoming data signal and the SDH container clock. Column 10, lines 2-4. Goodman further teaches that the FIFO receives inter-packet data for retiming. Column 10, lines 1-2. As understood by the Applicants, the Examiner is asserting that FIFO (element 490) is connected to a port scanning unit for storing data from all ports. However, there is no language in Goodman that teaches that the FIFO (element 490) is connected to a port scanning unit configured to extract data from ports providing data streams having at least two different input data rates. If the Examiner is asserting that the multiplexer (element 122) in Antosik teaches the port scanning unit, then the Examiner must provide a motivation and objective evidence for connecting FIFO (element 490) in Goodman to the multiplexer (element 122) as discussed above. Furthermore, there is no language in Goodman that teaches that the FIFO (element 490) receives data from ports. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 7 and 18, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Applicants further assert that Antosik and Goodman, taken singly or in combination, do not teach or suggest "temporarily storing data" as recited in claim 16. The Examiner has not cited to any passage in either Antosik or Goodman as teaching the above-cited claim limitation. The Examiner is reminded that in order to establish a *prima facie* case of obviousness, the Examiner has the initial burden of providing a prior art reference (or references when combined) that teach or suggest all of the claim limitations. M.P.E.P. §2142. Since the Examiner has not provided such evidence, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 16. M.P.E.P. §2142.

Applicants further assert that Antosik and Goodman, taken singly or in combination, do not teach or suggest "the step of temporarily storing data is provided according to the FIFO concept with a speed corresponding to the input data rate of the connected rate" as recited in claim 17. The Examiner has not cited to any passage in either Antosik or Goodman as teaching the above-cited claim limitation. The Examiner is reminded that in order to establish a *prima facie* case of obviousness, the Examiner has the initial burden of providing a prior art reference (or references when combined) that teach or suggest all of the claim limitations. M.P.E.P. §2142. Since the Examiner has not provided such evidence, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 17. M.P.E.P. §2142.

As a result of the foregoing, Applicants respectfully assert that there are numerous claim limitations not taught or suggested in the cited prior art, and thus the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 7 and 16-18. M.P.E.P. §2143.

III. ALLOWABLE SUBJECT MATTER:

Applicants thank the Examiner for the allowance of claims 23-28 and the indication of allowability of claims 4-6, 8-11, 15 and 19-22.

IV. CONCLUSION

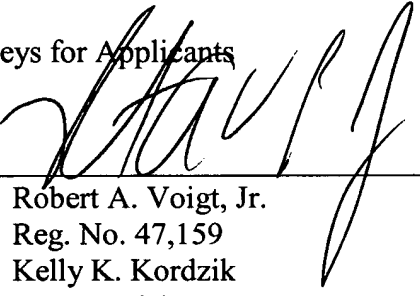
As a result of the foregoing, it is asserted by Applicants that claims 1-28 in the Application are in condition for allowance, and Applicants respectfully request an allowance of such claims. Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

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